


PAD FUNCTION

1. V_{OS} Trim
2. $-I_n$
3. $+I_n$
4. V^-
5. No Connect
6. Out
7. V^+
8. V_{OS} Trim

Backside (substrate)
 is an alloyed gold
 layer. Connect to V^- .

DIE CROSS REFERENCE

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
RH27C	RH27C DICE

DICE ELECTRICAL TEST LIMITS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	RH27C		UNITS
			MIN	MAX	
V_{OS}	Input Offset Voltage	(Note 1)		150	μV
I_{OS}	Input Offset Current			85	nA
I_B	Input Bias Current			90	nA
	Input Voltage Range		± 11.0		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11$	95		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	92		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k$, $V_O = \pm 10V$	600		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k$ $R_L \geq 600\Omega$	± 11.4 ± 10.0		V V
SR	Slew Rate	$R_L \geq 2k$	1.7		V/ μs
P_D	Power Dissipation			170	mW

Note 1. Input offset voltage measurements are performed by automatic equipment, approximately 0.5 seconds after application of power.

DICE SPECIFICATION

RH27

Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much "softer" than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move

the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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